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EXAMINER	
DSOUZA, JOSEPH FRANCIS A	
ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,108	BARRENSCHEEN ET AL.	
	Examiner	Art Unit	
	ADOLF DSOUZA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,18 and 20* is/are allowed.

6)☒ Claim(s) *1 - 16, 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Argument: Applicant amended claim 1 and then argued that the references did not disclose the new limitation.

Response: Examiner is introducing a new reference Flynn (US 5,525,971) that addresses the new limitation.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 4, 9 – 16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US 6,366,153) in view of Applicant Admitted Prior Art

(hereafter referred to as AAPA) and further in view of Ishii (EP_793111; which the Applicant has provided in his IDS (7/6/2004)) and Flynn (US 5,525,971).

Regarding claim 1, Arslain discloses an arrangement comprising:

a first semiconductor chip (Fig. 1, element 102) configured to transmit load control data (Fig. 1; column 2, lines 63 - 67; column 3, lines 1- 7);

and a second semiconductor chip connected coupled to the first semiconductor chip and (Fig. 1, element 100);

and a plurality of electrical loads coupled to the second semiconductor chip (Fig. 1, element 118)

wherein the second semiconductor chip is configured to:

a) drive the plurality of electrical loads based on a timing that is defined by the load control data (column 2, line 46 – column, line 7),

b) transmit to the first semiconductor chip diagnostic data which represent at least one of a plurality of states of the second semiconductor chip and events which occur in the second semiconductor chip (Fig. 1; column 3, lines 8 – 50).

Arslain does not disclose transmission of the load control data and pilot data, that the second semiconductor chip transmits the diagnostic data and that the load control data and pilot data are transmitted on a single line.

In the same field of endeavor, however, AAPA discloses the load control data and pilot control data (DATA2, DATA1a, Figure1) and the first semiconductor chip includes means for transmitting appropriate pilot data to the second semiconductor chip, and the second semiconductor chip includes means for controlling a transmission rate by which the diagnostic data is transmitted to the first semiconductor chip in accordance with the appropriate pilot data (Figure 1, DATA1b).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by AAPA, in the system of Arslain because this would allow for communication between the semiconductor chips.

In the same field of endeavor, however, Ishii discloses (c) control a transmission rate of the diagnostic data as prescribed by the pilot data (column 2, line 54 – column 3, line 4; wherein the pilot data is interpreted as the received initialization signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by Ishii, in the system of Arslain because this would allow the diagnostic data to be sent at the appropriate rate, as disclosed by Ishii.

In the same field of endeavor, however, Flynn discloses the load control data and pilot data are transmitted on a single line (column 5, line 27 – 36; wherein the single line is interpreted as the reduced width bus and the load control data and pilot data are interpreted as the data that are time multiplexed over the bus to reduce the number of lines).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Flynn, in the system of Arslain to time multiplex the load control data and pilot data because this would reduce the number of lines required, as disclosed by Ishii.

Regarding claim 2, Arslain discloses that the first semiconductor chip is a program-controlled unit (Fig. 1, element 102; wherein the program controlled unit is interpreted as the processor).

Regarding claim 3, Arslain discloses that the second semiconductor chip is a power chip (Fig. 1, element 100; wherein chip 100 is interpreted as the power chip).

Regarding claim 4, Arslain does not disclose that the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip.

In the same field of endeavor, however, Ishii discloses the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip, and wherein this transmission clock signal is not transmitted to the first semiconductor chip (Fig. 1, elements ECU and 20; column 2, line 54 – column 3, line 4; Fig. 4, bottom signal which is transmitted from the ECU to the diagnostic tester. The clock used to generate the bottom signal is not transmitted to the tester The second semiconductor chip is interpreted as the ECU unit and the first semiconductor chip is interpreted as the diagnostic tester).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by Ishii, in the system of Arslain because this would allow for data to be sent between the semiconductor chips without the clock signal being sent, thereby reducing the pin count and complexity.

Regarding claim 9, Arslain discloses the diagnostic data are transmitted via a line which transmits neither the load control data nor the pilot data are transmitted (Fig. 1; column 3, lines 8 – 33).

Regarding claim 10, Arslain discloses the load control data and the pilot data are transmitted via a transmission channel (Fig. 1).

Regarding claim 11, Arslain discloses the transmission channel comprises a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip (Fig. 1; column 2, line 63 - column 3, line 7), a data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal (Fig. 1; column 2, line 63 – column 3, line 7), and a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip (Fig. 1; column 2, line 63 – column 3, line 7).

Arslain does not disclose a chip select signal signaling to the second semiconductor chip the start and end of the transmission data.

In the same field of endeavor, however, AAPA discloses chip select signal signaling to the second semiconductor chip a start and end of the transmission of data intended for the second semiconductor chip via the data line ([0023]).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by AAPA, in the system of Arslain because this would allow for communication between the semiconductor chips.

Regarding claim 12, Arslain discloses the load control data and the pilot data are transmitted in units of frames, and are transmitted using time-division multiplexing (column 2, line 63 – column 3, line 7; wherein it is obvious that frames are used and that time division multiplexing is used).

Regarding claim 13, Arslain discloses the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a pilot data frame or no data (column 2, line 63 – column 3, line 7; wherein it is obvious to one of ordinary skill in the art that the transmission is in the form of windows).

Regarding claim 14, Arslain discloses the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where n>=0 and where n can be set by the user of the arrangement (column 3, lines 8 - 34).

Regarding claim 15, Arslain discloses a pilot data frame can be transmitted only in a time window in which no load control data frames is to be transmitted (column 2, line 63 - column 3, line 7).

Regarding claim 16, Arslain does not disclose transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

In the same field of endeavor, however, AAPA discloses transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously ([0009] – [0010]).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by AAPA, in the system of Arslain because this would allow for communication between the semiconductor chips.

Regarding claim 19, Arslain discloses the first semiconductor chip has a plurality of output drivers configured to output the load control data, the pilot data and the transmission clock signal (Figure 1; wherein it is obvious to one of ordinary skill in the art to increase the number of drivers).

5. Claim 5 - 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US 6,366,153) in view of Applicant Admitted Prior Art (hereafter referred to as AAPA) and further in view of Ishii (EP_793111; which the Applicant has provided in his IDS (7/6/2004) and Hastings et al. (US 6,772,251).

Regarding claim 5, Arslain does not disclose the transmission rate is prescribed by a transmitting a division factor.

In the same field of endeavor, however, Hastings discloses the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip divides the frequency of a transmission clock signal received from the first semiconductor chip by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant transmission signal (Fig. 1, element 122; column 1, lines 29 – 36; column 2, lines 60 – 67; column 3, lines 1 - 21).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by Hastings, in the system of Arslain because this would reduce the wire count (Hastings, column 1, lines 29 – 55).

Regarding claim 6, Arslain does not disclose the transmission clock signal transmitted to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

In the same field of endeavor, however, AAPA discloses the transmission clock signal supplied to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip ([0021] – [0025]).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by AAPA, in the system of Arslain because this would facilitate proper communication between the chips.

Regarding claim 7, Arslain does not disclose the diagnostic data are transmitted in units of frames, and each frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

In the same field of endeavor, however, Hastings discloses disclose the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values (Fig. 3, elements 310, 318).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by Hastings, in the system of Arslain because this would allow for a protocol for transmisison, as is obvious to one of ordinary skill in the art.

6. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arslain et al. (US 6,366,153) in view of Applicant Admitted Prior Art (hereafter referred to as AAPA) and further in view of Ishii (EP_793111; which the Applicant has provided in his IDS (7/6/2004).) and Jeong (US 5,675,584).

Regarding claim 8, Arslain does not disclose over sampling to determine the phase.

In the same field of endeavor, however, Jeong discloses the first semiconductor chip ascertains a phase of the diagnostic data by over sampling the diagnostic data (column 2, lines 62 – 65).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method , as taught by Jeong, in the system of Arslain because this would enable the phase of the incoming stream to be determined, as disclosed by Arslain.

Allowable Subject Matter

7. Claims 17, 18 and 20 are allowed.

8. Other Prior Art Cited

9. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to chip communication:

Hepworth et al. (US 3,975,712) discloses Asynchronous communication interface adaptor.

Fujii et al. (US 6,274,895) discloses a semiconductor integrated circuit device.

Fujii et al. (US 20020030212) discloses a semiconductor integrated circuit device.

Kobayashi et al (US 20020067638) discloses a semiconductor device and data processing system.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADOLF DSOUZA whose telephone number is (571)272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611